Amendments to the Claims:

There are no amendments to the claims. This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

10. (Previously presented) A duty cycle corrector circuit, comprising:

a first switch having a control input coupled to receive an input clock signal, the first switch being closed responsive to a first logic level of the input clock signal;

a second switch having a control input coupled to receive the input clock signal, the second switch being closed responsive to a second logic level of the input clock signal;

a first current regulating device coupled in series with the first switch between a first supply voltage and an output node, the first current regulating device having a control input coupled to receive a first control signal;

a second current regulating device coupled in series with the second switch between the output node and a second supply voltage; the second current regulating device having a control input coupled to receive a second control signal;

a capacitor coupled to the output node;

a level detector coupled to the output node, the level detector setting an output clock signal to a first logic level responsive to the voltage on the capacitor being greater than a first transition voltage and setting the output clock signal to a second logic level responsive to the voltage on the capacitor being less than a second transition voltage;

a third switch coupled in parallel with the first current regulating device, the third switch being structured to close responsive to the voltage on the capacitor being charged to at least the first transition voltage; and

a fourth switch coupled in parallel with the second current regulating device, the fourth switch being structured to close responsive to the voltage on the capacitor being discharged to at least the second transition voltage.

11. (original) The duty cycle corrector circuit of claim 10 wherein the first and second current regulating devices comprise respective first and second transistors having their gates coupled to receive the first and second control signals, respectively.

Claim 12 (cancelled).